PROPOSED CLAIMS FOR EXAMINER'S AMENDMENT

1. (Currently Amended) A memory device allowing charges accumulated in capacitors of a plurality of memory cells connected to a plurality of activated word lines to be combined along one bit line, the device comprising:

activation means for activating the plurality of word lines simultaneously; and

signal output means for outputting a digital signal having a value that corresponds to a total amount of charges obtained along the one bit line by combining the charges accumulated in the capacitors of the plurality of memory cells connected to the plurality of word lines activated by the activation means,

wherein the plurality of memory cells connected to the one bit line includes cells having different maximum predetermined capacitance of their capacitors.

2. (Original) The memory device according to claim 1, wherein the signal output means has:

voltage conversion means for converting the total amount of charges into a voltage signal that corresponds to this total amount of charges; and

analog-to-digital conversion means for converting the voltage signal obtained through conversion by the voltage conversion means from an analog signal into a digital signal.

3. (Cancelled).

4. (Original) The memory device according to claim 1, wherein the activation means simultaneously activates a plurality of word lines related to at least two items of data.

5. (Original) The memory device according to claim 4,

wherein, when one item of data has N number of bits (N: positive integer), N number of word lines related to this one item of data are used; and

wherein capacitors of N number of memory cells connected to the N number of word lines have capacitance that corresponds to weight of each bit of the data having the N number of bits.

6. (Original) The memory device according to claim 4, wherein data to be added is stored in a unit comprised of a plurality of memory cells connected to a plurality of word lines related to each item of data.

7. (Original) The memory device according to claim 4, wherein minuend data or subtrahend data is stored in a unit comprised of a plurality of memory cells connected to a plurality of word lines related to each item of data.

8. (Original) The memory device according to claim 7, wherein the minuend data is given in straight binary format and the subtrahend data is given in two's complement format.

9. (Currently Amended) A memory device comprising:

a first frame memory portion including a plurality of memory cells connected to bit lines and word lines, respectively, and arranged in a matrix, to store an image signal of a first frame; and

a second frame memory portion including a plurality of memory cells connected to the bit lines and word lines, respectively, and arranged in the matrix, to store an image signal of a second frame,

wherein the first frame memory portion and the second frame memory portion are formed consecutively in a row direction, in which the bit lines extend;

wherein, in the first frame memory portion and the second frame memory portion, charges accumulated in capacitors of a plurality of memory cells connected to a plurality of activated word lines can be combined along one bit line, the plurality of memory cells connected to the one bit line including cells having different maximum predetermined capacitance of their capacitors;

wherein, in each of the first frame memory portion and the second frame memory portion, [[a]] the plurality of memory cells connected to each of the bit lines is divided into units, each including a predetermined number of memory cells that are connected to a predetermined number of word lines, to store one item of pixel data in each of these divided units;

wherein each unit of the first frame memory portion stores pixel data of [[an]] the image signal of the first frame in straight binary format and each unit of the second frame memory portion stores pixel data of [[an]] the image signal of the second frame in two's complement format, and

wherein the memory device further comprises:

activation means for simultaneously activating a plurality of word lines related to predetermined data in the first frame memory portion and a plurality of word lines related to predetermined data in the second frame memory portion;

bit line selection means for selecting any one of the plurality of bit lines; and

signal output means for outputting a digital signal having a value that corresponds to a total amount of charges obtained along the bit line selected by the bit line selection means.

10. (Original) The memory device according to claim 9, further comprising saving means for saving pixel data of one line, the pixel data being stored in the first frame memory portion and the second frame memory portion, respectively, in accordance with the word lines activated by the activation means.

11. (Currently Amended) The memory device according to claim 9, further comprising storage position moving means for moving in a column direction a storage position of the pixel data stored in the first frame memory portion or the second frame memory portion.

12. (Currently Amended) The memory device according to claim 9, wherein, when the one item of pixel data has N number of bits (N: positive integer), N number of word lines related to this one item of pixel data are used, and capacitors of N number of

memory cells connected to the N number of word lines have capacitance that correspond to weight of each bit of the data having N number of bits.

13. (Currently Amended) A memory device comprising:

a memory portion including a plurality of memory cells connected to bit lines and word lines, respectively, and arranged in a matrix,

wherein, in the memory portion, charges accumulated in capacitors of a plurality of memory cells connected to a plurality of activated word lines can be combined along one bit line, the plurality of memory cells connected to the one bit line including cells having different maximum predetermined capacitance of their capacitors; and

wherein, in the memory portion, [[a]] the plurality of memory cells connected to each of the bit lines is divided into units, each including a predetermined number of memory cells that are connected to a predetermined number of word lines, to store one item of data in each of these divided units,

the memory device further comprising:

activation means for simultaneously activating word lines related to plural items of data;

bit line selection means for selecting any one of the plurality of bit lines; and

signal output means for outputting a digital signal having a value that corresponds to a total amount of charges obtained along the bit line selected by the bit line selection means.

14. (Currently Amended) The memory device according to claim 13, wherein, when the one item of data has N number of bits (N: positive integer), N number of word lines related to this one item of data are used, and capacitors of N number of memory cells connected to the N number of word lines have capacitance that corresponds to weight of each bit of the data having N number of bits.

15. (Currently Amended) The memory device according to claim 13,

wherein the memory portion has units as many as a number that corresponds to a plurality of pixel positions in one frame in a row direction, in which the bit lines extend, and units as many as a number that corresponds to search positions in a column direction, in which the word lines extend;

wherein a plurality of units of each row in the memory portion stores data of an absolute difference value between pixel data of a pixel ~~positions~~ position in a reference frame and pixel data of each of the search positions of a search frame correspondingly; and

wherein the activation means simultaneously activates word lines related to a unit that corresponds to a pixel position of each of the pixels that constitute a reference block of the reference frame.

16-19. (Cancelled).

20. (New) A memory device allowing charges accumulated in capacitors of a plurality of memory cells connected to a plurality of activated word lines to be combined along one bit line, the device comprising:

an activation unit configured to activate the plurality of word lines simultaneously; and

a signal output unit configured to output a digital signal having a value that corresponds to a total amount of charges obtained along the one bit line by combining the charges accumulated in the capacitors of the plurality of memory cells connected to the plurality of word lines activated by the activation unit,

wherein the plurality of memory cells connected to the one bit line includes cells having different maximum predetermined capacitance of their capacitors.

21. (New) A memory device comprising:

a first frame memory portion including a plurality of memory cells connected to bit lines and word lines, respectively, and arranged in a matrix, and configured to store an image signal of a first frame; and

a second frame memory portion including a plurality of memory cells connected to the bit lines and word lines, respectively, and arranged in the matrix, and configured to store an image signal of a second frame,

wherein the first frame memory portion and the second frame memory portion are formed consecutively in a row direction, in which the bit lines extend;

wherein, in the first frame memory portion and the second frame memory portion, charges accumulated in capacitors of a plurality of memory cells connected to a plurality

of activated word lines are configured to be combined along one bit line, the plurality of memory cells connected to the one bit line including cells having different maximum predetermined capacitance of their capacitors;

wherein, in each of the first frame memory portion and the second frame memory portion, the plurality of memory cells connected to each of the bit lines is divided into units, each including a predetermined number of memory cells that are connected to a predetermined number of word lines, and configured to store one item of pixel data in each of these divided units;

wherein each unit of the first frame memory portion is configured to store pixel data of the image signal of the first frame in straight binary format and each unit of the second frame memory portion is configured to store pixel data of the image signal of the second frame in two's complement format, and

wherein the memory device further comprises:

an activation unit configured to simultaneously activate a plurality of word lines related to predetermined data in the first frame memory portion and a plurality of word lines related to predetermined data in the second frame memory portion;

a bit line selection unit configured to select any one of the plurality of bit lines; and

a signal output unit configured to output a digital signal having a value that corresponds to a total amount of charges obtained along the bit line selected by the bit line selection unit.

22. (New) A memory device comprising:

a memory portion including a plurality of memory cells connected to bit lines and word lines, respectively, and arranged in a matrix,

wherein, in the memory portion, charges accumulated in capacitors of a plurality of memory cells connected to a plurality of activated word lines are configured to be combined along one bit line, the plurality of memory cells connected to the one bit line including cells having different maximum predetermined capacitance of their capacitors; and

wherein, in the memory portion, the plurality of memory cells connected to each of the bit lines is divided into units, each including a predetermined number of memory cells that are connected to a predetermined number of word lines, and configured to store one item of data in each of these divided units,

the memory device further comprising:

an activation unit configured to simultaneously activate word lines related to plural items of data;

a bit line selection unit configured to select any one of the plurality of bit lines; and

a signal output unit configured to output a digital signal having a value that corresponds to a total amount of charges obtained along the bit line selected by the bit line selection unit.